samtec

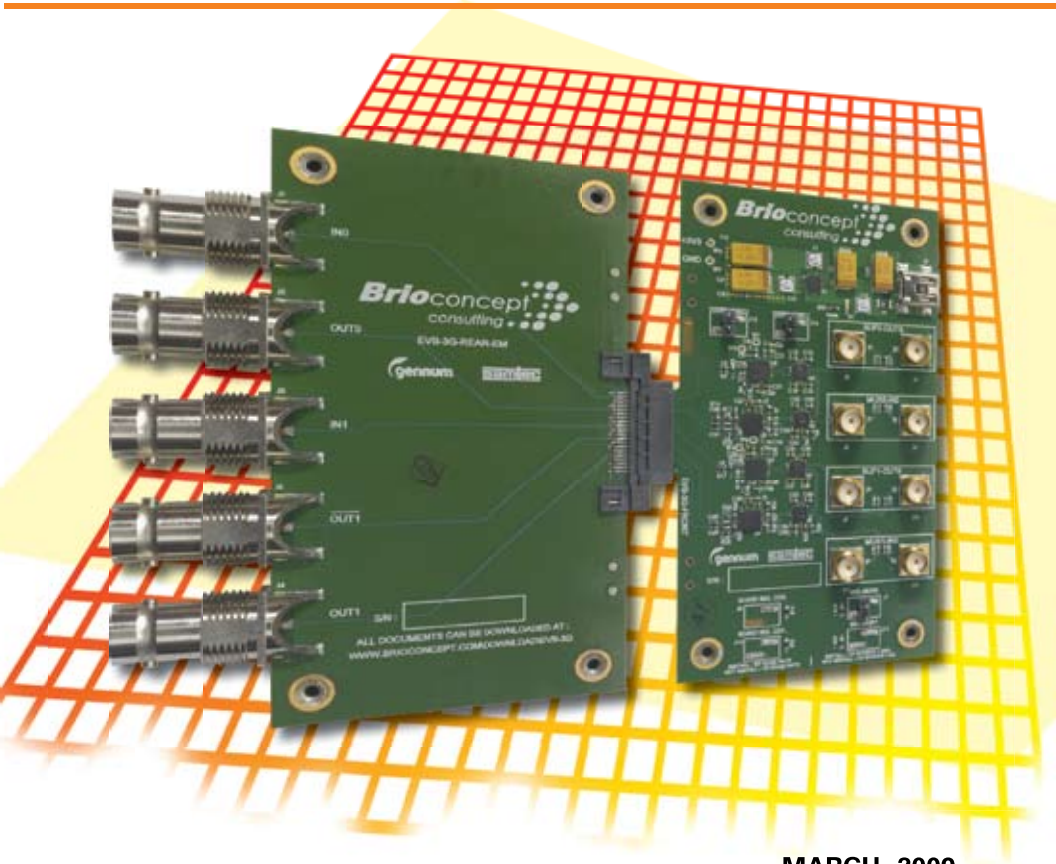
FinalInch®

Patent Pending

Test and Evaluation Kit User's Guide

FI-3G SDI-01

SIGNAL INTEGRITY DIVISION



MARCH 2009

Covering:

3G SDI Evaluation Board Set

Developed in conjunction with

Brioconcept consulting

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INTRODUCTION

Introduction

This 3G SDI Test and Evaluation Kit has been designed by Brioconcept consulting in collaboration with Samtec and Gennum. It has been created to demonstrate to video broadcast business OEMs how to develop a reliable design with Samtec's video BNC connector and Gennum's equalizer and cable driver. The boards also represent a real case design where the BNC connectors interface is permanently attached to an enclosure, and a hot-swappable active processing module is connected to it.

Finally, this kit is part of Samtec's commitment to provide integrated services for selection, development, simulation and testing of high speed systems. This guide was developed to help you to get the most out of these evaluation test boards.

Kit Contents

- One passive test card with edge mount 75Ω BNC (BNC7T-J-P-HN-ST-EM1) and one HSEC8-EM Series (HSEC8-120-01-S-D-EM2) connector to mate with the active card
- One passive test card with straight 75Ω BNC (BNC7T-J-P-HN-ST-TH1), right angle 75Ω BNC (BNC7T-J-P-HN-RA-BH1), and one HSEC8-EM Series (HSEC8-120-01-S-D-EM2) connector to mate with the active card
- One active test card populated with two Gennum equalizers (GS2974B) and two Gennum cable drivers (GS2978)
- One User's Guide (this document)
- One Application Note
- One USB cable to power-up the active card
- One wall mount power supply

3G SDI Evaluation Board complete kit.

Terms Used In This Guide

BOR: Breakout Region. The area close to the connector used for pad escape, via placement, and routing. See the Kit Features and overview sections for more details.

DUT: Device Under Test.

TDR: Time Domain Reflectometry. Time Domain Reflectometry is the analysis of a conductor (wire, cable, or fiber optic) by sending a pulsed signal into the conductor, and then examining the reflection of that pulse.

TDT: Time Domain Transmission. TDT measurements are made by passing an edge through the test device. Parameters typically measured are gain and propagation delay. Transmission measurements also characterize crosstalk between traces.

VNA: Vector Network Analyzer. The Vector Network Analyzer is an instrument used to measure the reflection and transmission properties of a signal in the frequency domain.

RL: Return Loss. Return Loss or Reflection Loss is the reflection of signal power resulting from the insertion of a device in a transmission line. It is usually expressed as a ratio in dB relative to the transmitted signal power.

3G SDI: 3G SDI is the serial digital interface for the uncompressed 1080p. The refresh rate could be 60 Hz, 59.94 Hz and 50 Hz. The nominal bitrates are: 2.97Gbps and 2.97Gbps/1.001. For more information, consult the standard SMPTE-424m.

HD-SDI: HD-SDI is the serial digital interface for the uncompressed 1080i, 720p. The refresh rate could be 60 Hz, 59.94 Hz and 50 Hz. The nominal bitrates are: 1.485Gbps and 1.485Gbps/1.001. For more information, consult the standard SMPTE-292m.

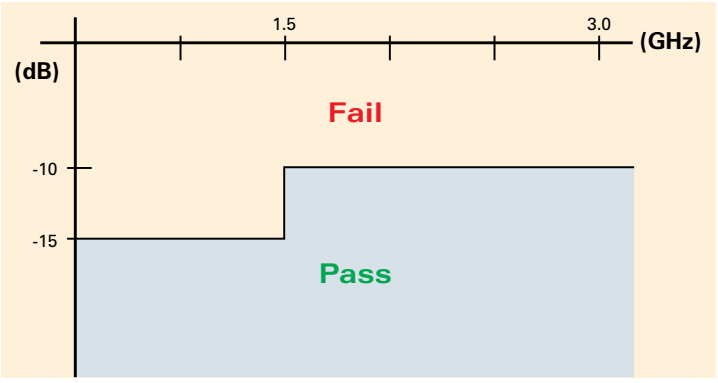
SD-SDI: SD-SDI is the serial digital interface for the uncompressed 525i, 625i. The refresh rate could be 60 Hz, 59.94 Hz and 50 Hz. The most popular bitrate is 270Mbps. For more information, consult the standard SMPTE-259m.

Design Features

This 3G SDI Test and Evaluation Board is based on the recommended layout documentation for the BNC connector and the high bandwidth SMA connector. The board itself is based on the simulation done by Brioconcept consulting with the connector models from Samtec and the Gennum's QFN package geometries. All the simulations have been executed with HFSS simulation software. The design has been optimized with high speed performance, affordable manufacturing processes, and standard materials in mind.

This evaluation board is exceptionally accurate when it comes to measuring signal quality in the connector breakout regions. Because the influence of a connector does not end at the printed circuit board, many connector systems have failed to deliver the high performance they claimed. In Final Inch® philosophy, the printed circuit board, breakouts, vias, traces, and active components are all considered an extension of the connector. As such, they are considered and designed in conjunction with the connector. Great care must be exercised when trading off electrical performance for PCB manufacturability. The PCB stack up and materials, via and pad size and location, trace designs, and active parts decoupling must all be carefully considered. If great care is not taken, the signal degradation caused in the break out region can be more significant than the one caused by the connector itself.

The boards represent a real case design where the BNC connectors interface is permanently attached to the enclosure, and a hot-swappable active processing module is connected to it. This scenario represents a stressful case where the SMPTE-424m return loss spec should be respected, even with those two connectors in the signal path. The following figure represents the SMPTE Return Loss curve.



Return Loss SMPTE curve.

INTRODUCTION *cont.*

To be SMPTE compliant for the Return Loss, the input/output Return Loss shall be under the curve. In fact, the signal shall have a minimum of -15 dB from DC to 1.5GHz and -10 dB from 1.5 GHz to 3 GHz.

The purpose of these designs is to help Samtec customers get a leg up on this critical video front end for the 3G SDI, HD-SDI, and SD-SDI signals. The system electrical performance has been evaluated and optimized through signal integrity modeling, simulations, and measurements. The test boards in this kit are just one portion of the complete Final Inch® package. Physical models of these designs in Gerber and schematics are available for cut and paste application into a customer's system design. Electrical models of the connector are available for cut and paste application into a customer's system signal integrity simulation tools. Due to confidential information, the models for the QFN package are available upon request.

To help customers to get to market faster, Samtec will grant license to Final Inch® designs. Contact finalinch@samtec.com for more information. For more information about physical art, simulation, and results, please contact Brioconcept consulting at info@brioconcept.com

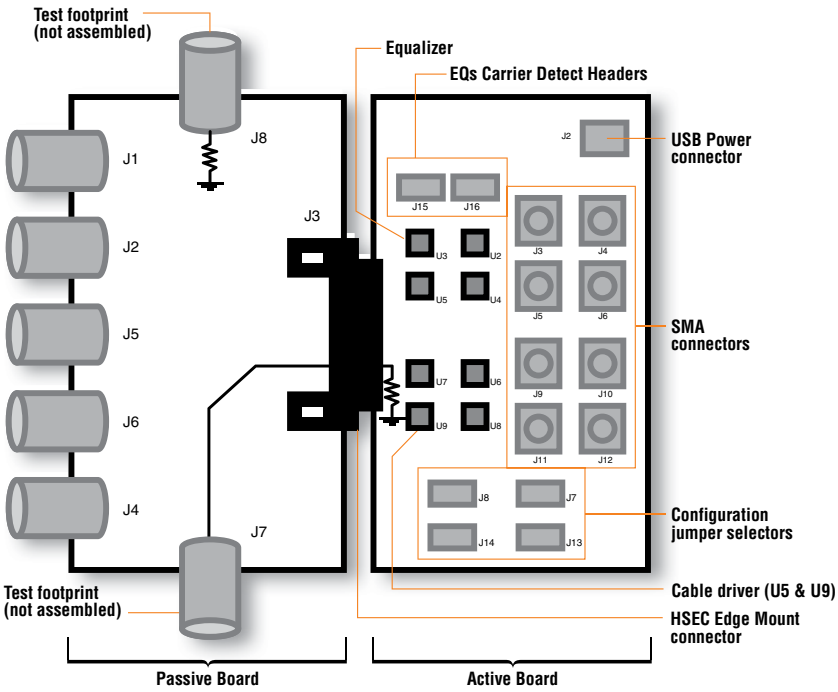
OVERVIEW

Evaluation Kit Description

The 3G SDI Test and Evaluation Board contains three boards: two passives and one active.

The passive boards contain only connectors and represent the interface permanently attached to the enclosure in a multi-board system. The kit contains two passive boards to provide the most flexible way to characterize the three different Samtec BNCs. The first board features Edge Mount connectors, and the other one is assembled with both Right Angle and Straight BNCs. Two BNC footprints are available (J7 & J8) for static load testability. J8 is connected to the load via the shortest possible trace, and J7 is connected to a load on the active board via a long trace and the HSEC8 Series connector (see Application Note for more information). The two passive boards are fully interchangeable and will be referred to independently in this document as "the passive board".

The active board contains the Gennum equalizers and cable drivers. It is used to interface discrete or FPGA Serializer / Deserializer with the SMA connectors. It represents the typical front end of a hot-swappable processing module in a multi-board system.



3G SDI Evaluation Boards overview.

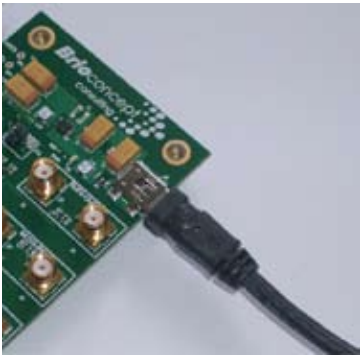
OVERVIEW *cont.*

Quick Start

1. Connect one of the passive boards with the active board.

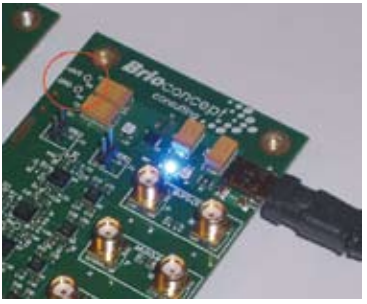
Passive/Active boards

2. Connect the USB Power cable into the J2 connector of the active board. Connect the other extremity of the USB cable to any computer or optionally use the included AC/DC USB adaptor to power it from an AC outlet.



USB plug connection

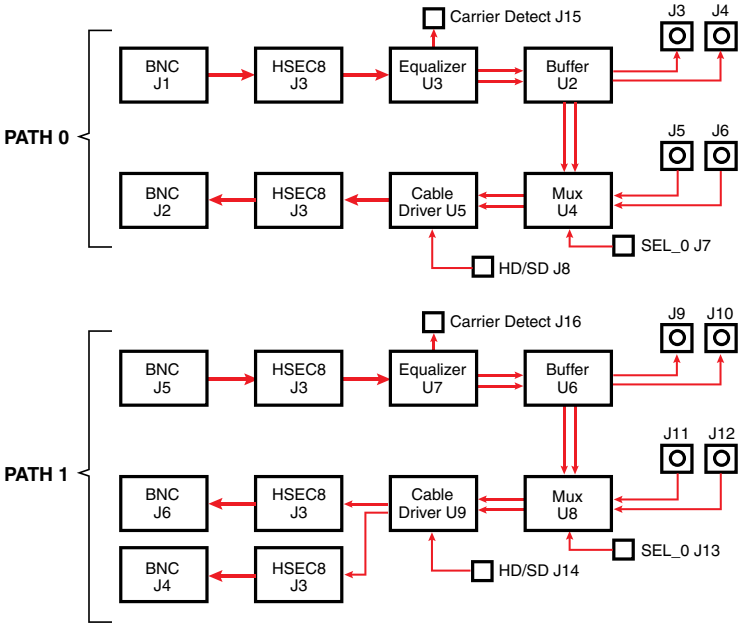
3. When the blue led light is on, the board is ready to be used. In addition, you can probe the power supply output on the provided test pads (TP6 = 3.3 volts and TP7 = GND).



LED power on indicator & Power supply test pads

Test Configurations

This 3G SDI Test and Evaluation Board Kit has been designed to test the multiple configurations usually seen by broadcast video equipment designers. The following figure shows a block diagram of the 3G SDI Evaluation Board.



3G SDI Evaluation Board block diagram

Basically, the 3G SDI Evaluation Board is divided into two independent paths. Both paths include an Equalizer and a Cable Driver. The input for the Equalizer is coming from a BNC, and this output signal can simply be sent out of the Evaluation Board through the SMA connectors or be looped-back to the Cable Driver. The Cable Driver's input can be selected from SMA connectors or from the Equalizer output. On Path 0, the Cable Driver's output is routed to a single BNC. But on the Path 1, the Cable Driver outputs the signal and the complement of the signal to two distinct BNCs. In addition, the headers J15 and J16 give access to the Equalizer's Carrier Detect signal for the Path 0 and Path 1 respectively. Pay attention to the Carrier Detect signal when REV B (GS2974B) of the equalizer is installed*.

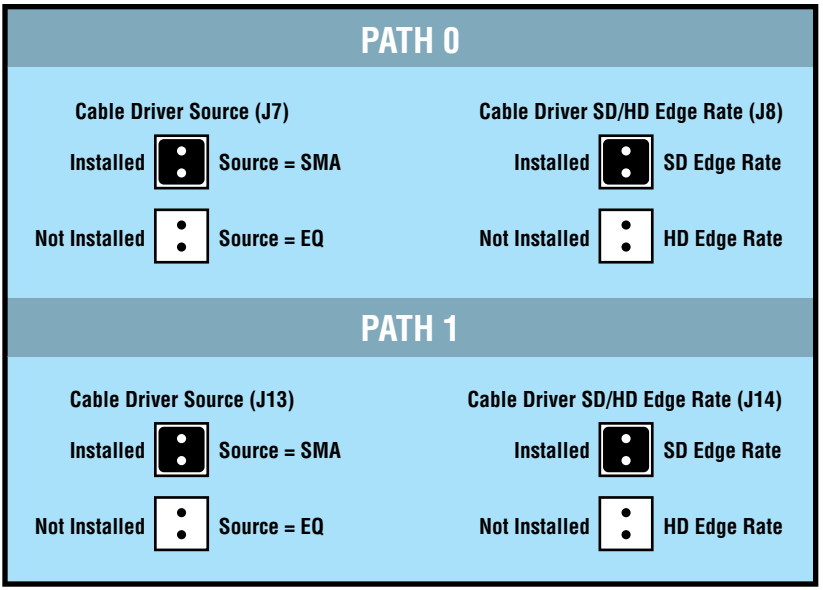
* The GS2974B (REV B) input stage is more sensible than the GS2974A (REV A). It could do false carrier detection in a noisy environment. As both Rev A and Rev B Equalizers are pin compatible, you should prefer to have REV A installed on the active board if your application needs accurate carrier detection.

OVERVIEW *cont.*

Three useful configurations are available for test through the jumper's configuration:

1. Loopback
2. Deserializer
3. Serializer

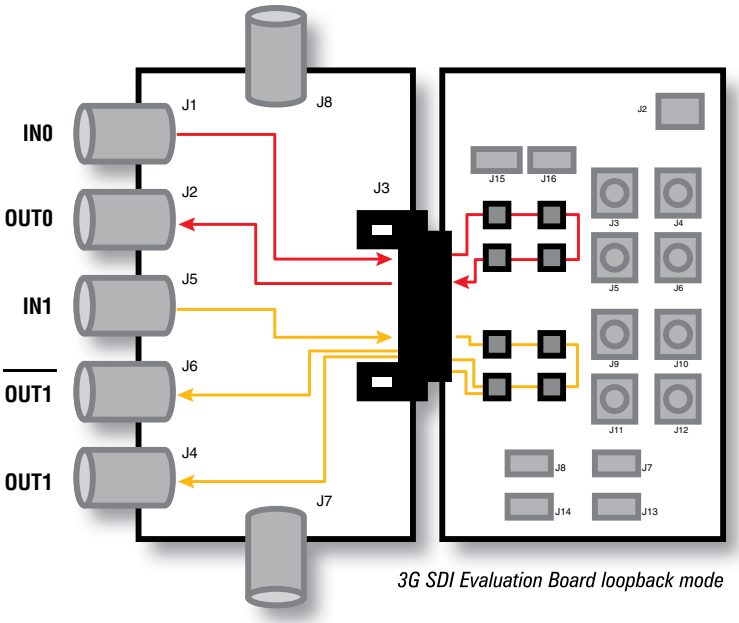
Jumpers J13 and J14 are used to configure Path 0 and J7 and J8 are used to configure Path 1. The following table shows the jumper's configurability.



3G SDI Evaluation Board configuration jumpers

1. Loopback (default)

In this mode, the signal is coming from the input BNC. It passes through the Equalizer, and then is looped-back to the Cable Driver. Finally, the output signal is routed to the output BNC(s). On the Path 1, the signal's complement is also available*. You can select between SD or HD edge rate with the jumpers J8 and J14 for Path 0 and Path 1 respectively. The Loopback HD is the default configuration when no jumper is present.



3G SDI Evaluation Board loopback mode

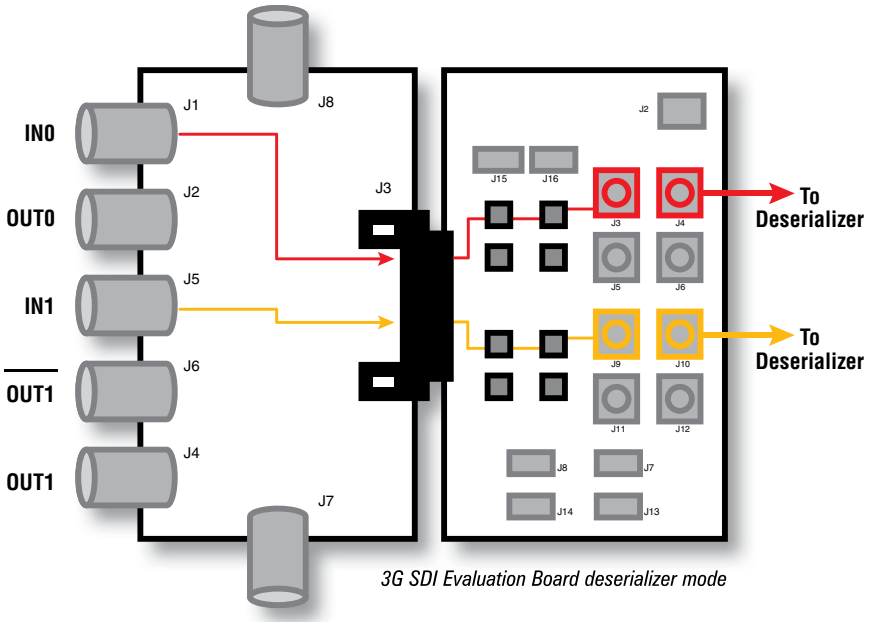
	PATH 0		PATH 1	
	J8	J7	J14	J13
SD	Installed	Not Installed	Installed	Not Installed
HD	Not Installed	Not Installed	Not Installed	Not Installed

3G SDI Evaluation Board loopback mode jumper's configuration

* DVB ASI is not supported on the Path 0 due to voluntary pair inversion on the board to simplify the routing. The DVB ASI is supported on Path 1 by using the complementary output (/OUT1).

2. Deserializer

In this mode, the signal is coming from the input BNC. It passes through the Equalizer, and then is outputted through the SMA connectors. A discrete or FPGA deserializer is usually connected to those SMAs for processing purposes. You can select between SD or HD edge rate with the jumpers J8 and J14 for Path 0 and Path 1 respectively. The loopback mode is still available depending on the jumpers (J7 & J13) positions. Test equipment could be attached to this looped-back signal (BNC) to validate the behavior of the deserializer.



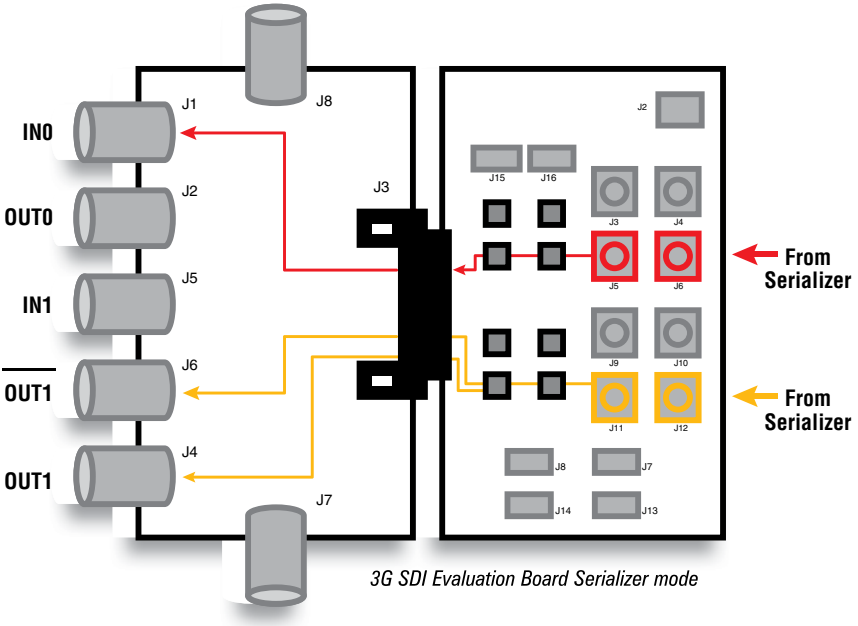
3G SDI Evaluation Board deserializer mode

	PATH 0		PATH 1	
	J8	J7	J14	J13
SD	Installed	Don't Care?	Installed	Don't Care?
HD	Not Installed	Don't Care?	Not Installed	Don't Care?

3G SDI Evaluation Board deserializer mode jumper's configuration

3. Serializer

In this mode, the signal is coming from the input SMA. It passes through the Cable Driver, and then is output through the BNC connectors. On the Path 1, the signal's complement is also available. You can select between SD or HD edge rate with the jumpers J8 and J14 for Path 0 and Path 1 respectively. The Equalized signal that is coming from the input BNC is still available on the output SMA. This enables a processing block to be used between the Equalizer and the Cable Driver.



3G SDI Evaluation Board Serializer mode

	PATH 0		PATH 1	
	J8	**J7**	**J14**	**J13**
SD	Installed	Installed	Installed	Installed
HD	Not Installed	Installed	Not Installed	Installed

3G SDI Evaluation Board serializer mode jumper's configuration

DUT MEASUREMENTS

Recommended Test Equipment

Brioconcept consulting and Gennum used the following test equipment to characterize the evaluation boards:

- Frequency Domain Measurements of Return Loss:
  - Network Analyzer HP 8753C 300kHz-6GHz
  - S-parameter set HP 85047A 300kHz-6GHz
  - Calibration Kit Maury Microwave Corp. 8580A 75ohms

Network Analyzer HP 8753C

- TDR/TDT Time Domain Measurements:
  - Tektronix 11801C Digital Sampling Oscilloscope with an SD-24 TDR/Sampling Head

Tektronix 11801C

Test Equipment Accuracy Issues

In any measurement system, there are three issues that need to be addressed: Test Equipment Accuracy, Test Fixture Effects, and the characteristics of the Device under Test (DUT).

Test Equipment Accuracy

Oscilloscopes, Vector Network Analyzers (VNA), current meters, etc. each have inherent errors associated with them. Each has a finite bandwidth, noise floor, linearity, drift, etc. that affects the final accuracy of the measurement. Some of these characteristics can be calibrated out, some cannot. Each instrument will measure to within a certain percentage of the actual input signal.

Improvements in the accuracy of measurement can be had by calibration and/or by applying correction factors to the measurements.

Other inherent characteristics of the equipment cannot be eliminated. Random noise, drifts over time, temperature, humidity, non-repeatable connections, etc. cannot be eliminated, but can be reduced by good operating procedures. There are also limitations in the practical accuracy of the calibration standards applied.

Test Fixture Effects

Test Fixtures add their own set of bandwidth filtering, noise, impedance discontinuities, resonances, and other errors to the overall uncertainty of the measurements. A test board used to connect to the connectors has dielectric losses, imperfect Zo, skin effect losses, crosstalk, etc. The connection between the DUT and the test equipment is never perfect resulting in reduced bandwidth, added aberrations, and/or additional noise.

Characteristics of the DUT

The Device Under Test has its own set of issues. First, the contact between the HSEC8 Series connector and the gold fingers should be well connected to ensure a good signal path. Will the characteristic of interest be swamped out by limitations in the test equipment? Whenever you measure the DUT, you are disturbing it.

Earlier in this guide, we discussed at length how Samtec and Brioconcept consulting have eliminated or greatly reduced the effects of the last two issues leaving only the test equipment as a potential source of errors that could greatly affect the final accuracy of the measurement. The following section describes a procedure to follow that will help improve the accuracy of measurement through calibration using the BNC 75Ω evaluation board Final Inch® Test Trace Board.

Measurement Techniques

Brioconcept consulting recommends two complementary measurement techniques to characterize the Evaluation Board: TDR/TDT for Time Domain and VNA for the Frequency Domain.

DUT MEASUREMENTS *cont.*

Frequency Domain Measurements

Calibration

Before the measurements of the connectors can be made, a full 1-port calibration of the VNA should be performed with the 75Ω calibration kit. The calibration constants should be stored and be applied to all measurements of the Evaluation Board. Thus, any deviation from an ideal set of measurements using this calibration will result solely from the characteristics of the Evaluation Board.

Time Domain Measurements

Brioconcept consulting and Gennum used a Tektronix TDS8000 with 80E03 equipped with a 20 GHz sampling head and 80E04 20 GHz sampling head/TDR to characterize the connectors in the Time Domain. The 80E04 is used for TDR characterization and in conjunction with the 80E03 for TDT characterization. See the Application Note for more results in Time Domain and Frequency Domain.

REFERENCE MATERIALS

Related Documentation Available

At the beginning of this guide, we mentioned that the Test and Evaluation Boards included in this Kit have been manufactured and characterized through measurements and then correlated to simulations. All results are available for customer review and use including:

- Recommended Layout Documentation.
- CAD importable Gerber and DXF files.
- Test Board Application Notes and Characterization Reports.

Contacts

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Recommended Reading

Primer - "A Digital Designer's Guide to Verifying Signal Integrity,"

Tektronix Inc. ftp://ftp.tek.com/mbd/software/misc/TEK_PRIM_FINAL.PDF

Primer – "Understanding the Fundamental Principals of Vector Network Analysis," Agilent, Inc. document AN 1287-1 http://cp.literature.agilent.com/litweb/pdf/5965-7707E.pdf

App Note – "TDR Impedance Measurements: A Foundation for Signal Integrity," Tektronix Inc. http://www.tek.com/Measurement/App_Notes/55_14601/eng/ 55W_14601_0.pdf

Web Sites:

www.brioconcept.com

www.gennum.com

www.samtec.com

NOTES

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